Shri Vile Parle Kelavani Mandal's

Dwarkadas J. Sanghvi College of Engineering

(Autonomous College Affiliated to the University of Mumbai)

Scheme and detailed syllabus (DJ19)

Third Year B. Tech.

in

Electronics & Telecommunication Engineering

(Semester V)

Revision: 1 (2019)
With effect from the Academic Year: 2021-2022

1st July, 2021

SEMESTER V

Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

Scheme for Third Year Undergraduate Program in Electronics & Telecommunication Engineering : Semester V (Autonomous) (Academic Year 2021-2022)

Sem V

Sr	Course Code	Course	Teaching Scheme				Semester End Examination (A)						Continuous Assessment (B)					Aggregate (A+B)	Credits earned	
			Theory (hrs.)	Practical (hrs.)	Tutorial (hrs.)	Credits	Duration (Hrs)	Theory	Oral	Pract	Oral & Pract	SEE Total (A)	Term Test 1 (TT1)	Term Test 2 (TT2)	Avg (TT1 & TT2)	Term Work Total	CA Total (B)			
1	DJ19ECC501	Microprocessor & Microcontroller	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	4
	DJ19ECL501	Microprocessor & Microcontroller-Laboratory	--	2	--	1	2	--	--	--	25	25	--	--	--	25	25	50	1	
2	DJ19ECC502	Digital Signal Processing	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	4
	DJ19ECL502	Digital Signal Processing -Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
3	DJ19ECC503	Radio Frequency Circuit Design	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	4
	DJ19ECL503	Radio Frequency Circuit Design - Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
4@	DJ19ECEC5011	Control Systems	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	4
	DJ19ECEL5011	Control Systems - Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
	DJ19ECEC5012	Computer Organization & Architecture	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	
	DJ19ECEL5012	Computer Organization & Architecture - Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
	DJ19ECEC5013	Basic VLSI	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	
	DJ19ECEL5013	Basic VLSI -Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
	DJ19ECEC5014	Neural Network & Fuzzy Logic	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	
	DJ19ECEL5014	Neural Network & Fuzzy Logic - Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
	DJ19ECEC5015	Operating Systems	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	
	DJ19ECEL5015	Operating Systems- Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
	DJ19ECEC5016	Power Electronics	3	--	--	3	3	75	--	--	--	75	25	25	25	--	25	100	3	
	DJ19ECEL5016	Power Electronics- Laboratory	--	2	--	1	--	--	25	--	--	25	--	--	--	25	25	50	1	
5	DJ19ECSBC1	Data Structures & Algorithms	2	--	--	2	3	75	--	--	--	75	25	25	25	--	25	100	2	3
	DJ19ECSBL1	Data Structures & Algorithms - Laboratory	--	2	--	1	--	--	--	--	--	--	--	--	--	25	25	25	1	
	DJ19ECSBL2	Database Management System - Laboratory	--	2	--	1	--	--	--	--	--	--	--	--	--	25	25	25	1	1
#6	DJ19IHL2	Professional & Business Communication - Laboratory	--	4	--	2	--	--	--	--	--	--	--	--	--	50	50	50	2	2
7	DJ19ILL1	Innovative Product Development-III	--	2	--	1	--	--		--	25	25	--	--	--	25	25	50	1	1
		Total	**14**	**18**	--	**23**	**17**	**375**	**75**	--	**50**	**500**	**125**	**125**	**125**	**225**	**350**	**850**	**23**	

@ Any 1 Elective Course

2 hrs. of theory (class wise) and 2 hrs of activity based laboratory (batch wise)

Prepared by | Checked by | **Head of the Department** | **Vice Principal** | **Principal**

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics and Telecommunication Engineering</td><td colspan="2">Semester: V</td></tr>
<tr><td colspan="8">Course: Microprocessor & Microcontroller</td><td colspan="2">Course Code: DJ19ECC501</td></tr>
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</table>

Pre-requisite:

1. Digital System Design

Objectives:

1. To develop background knowledge and core expertise in microcontrollers.
2. To understand peripheral devices and their interfacing to microcontrollers.
3. To write programs for microcontrollers and their applications in Assembly language.

Outcomes: On completion of the course, learner will be able to:

1. Identify different functionalities, hardware components and relevant programming software's for 8085 and 8051.
2. Write programs for 8051 microcontroller-based systems with the help of appropriate instruction set.
3. Interface different I/O's with 8051 microcontrollers for various applications.
4. Identify different functionalities and architecture of ARM 7.

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**8085 Architecture and Programming:** 8085 microprocessor architecture and its functional blocks,8085 microprocessor pin diagram.,8085 microprocessor Addressing modes, Instruction set.	**09**
2	**8051 Microcontroller:** Features, architecture and pin configurations, CPU timing, Input / Output ports, Memory organization, Counters and timers, Interrupts.	**10**
3	**8051 Programming:** Instruction set, Addressing mode, Assembler Directives **Programs related to**: arithmetic, logical, delay, input, output, timer, Counters, port, serial communication, and interrupts.	**10**
4	**Interfacing and Applications:** Interfacing of Display: LED, LCD and Seven Segment display, Stepper motor, Relay and UART.	**05**
5	**ARM7: A 32-bit Core Architecture:** Features of ARM core architecture, Data Flow Model, Pipeline, Registers, operating modes.	**05**

List of Laboratory Experiments: (minimum eight)

1. To find smallest and largest number from given data string using 8051.
2. To perform multi byte addition.
3. To exchange data blocks using 8051.
4. To generate waveform using 8051.
5. To interface 7-segment display with 8051.
6. To measure pulse width using 8051.
7. To transfer and receive data serially using 8051.
8. To interface key matrix with 8051.
9. To generate waveforms using DAC and 8051.
10. To display the message on LCD using 8051.

Books Recommended:

Text Books:

1. Ramesh S. Gaonkar, *Microprocessor - Architecture, Programming and Applications with the 8085*, 5th Edn, Penram International Publication.

2. Ajay Deshmukh, *Microcontrollers: Theory and Applications*, 6th Edn, Tata McGraw Hill Publication.
3. M. A. Mazidi, J. G. Mazidi and R. D. Mckinlay, *The 8051 Microcontroller & Embedded systems*, 2nd Edn, Pearson Publication.
4. Lyla Das, *Embedded Systems: An Integrated Approach*, 1st Edn, Pearson Publication.

Reference Books:

1. Brarry B. Bray, *The 8085A Microprocessor software, programming and Architecture*, 2nd Edn, Prentice Hall India Publication.
2. C. Kenneth J. Ayala and D. V. Gadre, *The 8051 Microcontroller & Embedded system Using Assembly and C*, 1st Edn, Cengage Learning Publication.
3. Andrew Sloss, Dominic Symes, and Chris Wright, *ARM System Developer's Guide : Designing and Optimizing System Software*, 1st Edn, Morgan Kaufmann Publication.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practical's performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments, and a case study based on any one topic is compulsory.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments, Case study): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
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Pre-requisite:

1. Signals and Systems

Objectives:

1. To develop a thorough understanding of DFT and FFT and their applications.
2. To teach the design techniques and performance analysis of digital filters
3. To introduce the students to digital signal processors and its applications.

Outcomes: On completion of the course, learner will be able to:

1. Implement DFT and FFT algorithms in finding the response of the system.
2. Design different types of IIR filters.
3. Design different types of FIR filters.
4. Determine effects of Poles and Zeros in the frequency response of digital filters.

Detailed Syllabus: unit wise		
Unit	**Description**	**Duration**
1	**Discrete Fourier Transform & Fast Fourier Transform:** Definition and Properties of DFT, IDFT, Circular convolution of sequences using DFT and IDFT. Filtering of long data sequences: Overlap-Save and Overlap-Add Method for computation of DFT. Fast Fourier Transforms (FFT), Radix-2 decimation in time and decimation in frequency FFT algorithms, inverse FFT, composite Radix FFT N=2.3, N=3.2.	**10**
2	**IIR Digital Filters:** Types of IIR Filters (Low Pass, High Pass, Band Pass, Band Stop), Analog filter approximations: Butterworth, Chebyshev I. Mapping of S-plane to Z-plane, impulse invariance method, bilinear transformation method, Design of IIR digital filters (Butterworth and Chebyshev-I) from Analog filters with numerical examples. Effect of Poles and Zeros on the Frequency Response of IIR filters. Position of Poles and Zeros of Low Pass, High Pass, Band Pass, Band Stop, All Pass filters.	**10**
3	**FIR Digital Filters:** Characteristics of FIR digital filters, Minimum Phase, Maximum Phase, Mixed Phase and Linear Phase (Type 1 to Type 4) FIR Filters. Design of FIR filters using Window techniques (Rectangular, Hamming, Hanning, Blackman, Kaiser), Design of FIR filters using Frequency Sampling technique, Comparison of IIR and FIR filters.	**08**
4	**Poles, Zeros and Filters:** Effects of poles and zeros in the frequency response of IIR filters (LP, HP, BP, BR/Notch, All Pass filters). Placement of zeros and design of filters in Type1 to Type 4 Linear Phase FIR filters. **Finite Word Length effects in Digital Filters** Quantization, truncation and rounding, Error due to truncation and rounding.	**06**
5	**DSP Processors:** Introduction to General Purpose and Special Purpose DSP processors, fixed point and floating-point DSP processor, Computer architecture for signal processing, Harvard Architecture, Pipelining, multiplier and accumulator (MAC), Special Instructions, Special purpose DSP hardware, Architecture of TMS320CX fixed and floating DSP processors.	**04**
6	**Applications of Digital Signal Processing:** Application of DSP for ECG signals analysis.	**04**

	Application of DSP for Dual Tone Multi Frequency signal detection. Application of DSP for Radar Signal Processing	

List of Laboratory Experiments: (minimum eight)

1. Plot of Discrete Time Signals.
2. Frequency response of LTI systems by DTFT.
3. To perform Discrete Fourier Transform.
4. To implement Circular Convolution of two discrete time sequences.
5. To perform Overlap Add method of DFT for long data sequence.
6. To implement the algorithm of DIT-Fast Fourier Transform.
7. To plot the FFT of Sinusoids with noise.
8. Magnitude and phase response of FIR filter.
9. Design an Analog Butterworth filter with given specifications.
10. Design a Digital IIR Butterworth filter with given specifications.
11. Design an FIR filter by window method.
12. Removal of Noise by a designed filter.

Books Recommended:

Text books:

1. J. Proakis and D. Manolakis, *Digital Signal Processing*, 4th Edn, Pearson Education.
2. A. Oppenheim, R. Schafer and J. Buck, *Discrete Time Signal Processing*, 2nd Edn, Pearson Education.
3. B. Venkata Ramani and M. Bhaskar, *Digital Signal Processors, Architecture, Programming and Applications*, 2004, Tata McGraw Hill.

Reference Books:

1. Emmanuel C. Ifeachor and Barrie W. Jervis, *Digital Signal Processing A Practical Approach*, 2nd Edn, Pearson Education.
2. Sanjit K. Mitra, *Digital Signal Processing – A Computer Based Approach*, 4th Edn, McGraw Hill Education (India) Private Limited.
3. Tarun Kumar Rawat, *Digital Signal Processing*, 2015, Oxford University Press.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practical performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments.

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ii. Journal Documentation (Write-up, Tutorials): 10 marks

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Pre-requisite:

1. Electromagnetics and Wave Propagation
2. Electrical Network Analysis and Synthesis
3. Applied Mathematics-III

Objectives:

1. To develop the model for inductor, capacitor and resistor at high frequency.
2. To analyse transmission line using Smith Chart
3. To study application of smith chart for impedance matching

Outcomes: On completion of the course, learner will be able to:

1. Apply their knowledge in analyzing behavior of inductor, capacitor and resistor at high frequency.
2. Calculate various parameters of transmission line analytically and using Smith Chart.
3. Design matching network using various techniques.
4. Design the filters for given specifications using insertion loss and image parameter method.
5. Analyze the single and Multi-port network using parameters.

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Single- and Multiport Networks:** **Basic Definitions** Interconnecting Networks, Series Connection of Networks, Parallel Connection of Networks, Cascading Networks. **The Scattering Matrix** Reciprocal Networks and Lossless Networks, A Shift in Reference Planes, Power Waves and Generalized Scattering Parameters, Practical Measurements of S-Parameters. **The Transmission (ABCD) Matrix** Relation to Impedance Matrix and Scattering Matrix, Equivalent Circuits for Two-Port Networks.	**06**
2	**Importance of Radio Frequency Design:** **RF behaviour of Passive Components** High-Frequency Resistors, High-Frequency Capacitors, High-Frequency Inductors. **Chip Components and circuit Board Considerations** Chip Resistors, Chip Capacitors, Surface-Mounted Inductors. **SMD Assembly Process** Solders for SMD Applications, Fluxing and Cleaning, Types of Flux- Organic Soluble Fluxes, R Flux, RMS Flux, RA Flux, Water Soluble Fluxes and Types Flux Selection, Solder Applications, Curing solder Paste, The Reflow Process, Assembly Methods, Adhesive Applications and Curing, Solder Creams.	**06**
3	**Smith Chart:** **From Reflection Coefficient to Load Impedance** Reflection coefficient in Phasor Form, Normalised Impedance Equation, Parametric Reflection Coefficient Equation, Graphical Representation. **Impedance Transformation** Impedance Transformation for General Load, Standing Wave Ratio, Special Transformation Conditions. **Admittance Transformation** Parametric Admittance Equation, Additional Graphical Displays. **Z-Y Smith Chart** **Parallel and Series Connection of Lumped Elements and their analysis using Smith Chart** Parallel Connection of R and L, Parallel Connection of R and C, Series Connection of R and L,	**10**

	Series Connection of R and C, T and π Network.	
4	**Impedance Matching and Tuning:** **Matching with Lumped Elements (L Networks)** Analytic Solutions, Smith Chart Solutions. **Impedance Transformers** Single-Section Quarter-Wave Transformer, Multi-section Quarter-Wave Transformer, Transformers with Uniformly distributed section reflection coefficient, Binomial Multi-section Matching Transformer, Chebyshev Multi-section Matching Transformer, Exact formulation and design of Multi-section Matching Transformer. **Tapered Lines** Exponential Taper, Triangular Taper, Klopfenstein Taper.	**10**
5	**RF Filter Design:** **Basic Resonator and Filter configurations** Filter Types and Parameters, Low-Pass Filter, High-Pass Filter, Bandpass and Bandstop Filters, Insertion Loss. **Special Filter Realizations using Insertion Loss Method** Butterworth-Type Filters, Chebyshev-Type Filters, Denormalization of Standard Low-Pass Design. **Filter Implementation** Unit Elements, Kuroda's Identities, Microstrip Filter Design. **Filter Design by the Image Parameter Method** Image Impedances and Transfer Functions for Two-Port Networks, Constant-k Filter sections, m-derived Filter Sections, Composite Filters.	**10**

List of Laboratory Experiments: (minimum eight)

1. Characterisation of resistor at high frequency
2. Characterisation of inductor and capacitor at high frequency
3. Analysis of Parallel and Series Connection of Lumped Elements and verification using Smith chart
4. Filter Design by the Image Parameter Method
5. Filter Design by the Insertion Loss Method
6. Matching of Lumped Elements
7. Design of quarter wave transformer
8. Design of Binomial Multi-Section Matching Transformer
9. Numerical from previous years GATE Examination paper.

Books Recommended:

Text books:

1. Ludwig, Reinhold & Bretchko, Pavel (2007*). RF circuit design: Theory and applications*, 2nd Edn, 2007, Prentice-Hall, N.J.
2. Pozar, David M., *Microwave Engineering*, 2012, Hoboken, NJ : Wiley Publication
3. Traister, John, *Design Guidelines for Surface Mount Technology*, 2012, Elsevier.

Reference books:

1. Guillermo Gonzalez., *Microwave transistor amplifiers*: *Analysis and design*, 1996, Prentice-Hall, Inc., USA.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practicals performed during laboratory sessions.

Continuous Assessment (B):

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Pre-requisite:

1. Engineering Mathematics-III & IV
2. Electrical Networks Analysis & Synthesis
3. Signals and Systems

Objectives:

1. To provide fundamental concept of control systems such as mathematical modelling, time response and frequency response of the system.
2. To develop concepts of stability and its assessment criteria of the system.
3. To study basic concepts of advanced control systems and servo motor.

Outcomes: On completion of the course, learner will be able to:

1. Understand the basic concepts of control system and develop the mathematical model.
2. Analysis of systems in time and frequency domain.
3. Analyze the stability of control systems using appropriate criteria.

4. Design the conventional controllers for industrial applications.
5. Gain ability to work in teams to solve complex problems and communicate effectively with technical reports / write-ups.

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Introduction to Control System Analysis:** Introduction: Open loop and closed loop systems, feedback and feed forward control structure, examples of control systems. Modeling: Types of models, impulse response model, state variable model, transfer function model. Dynamic Response: Standard test signals, transient and steady state behavior of first and second order systems, steady state errors in feedback control systems and their types.	**08**
2	**Mathematical Modeling of Systems:** Conversion of block diagram to signal Flow Graph and Vice-versa., Transfer Function models of various Electrical systems, Block diagram reduction for MIMO and SISO systems, signal flow graph, Mason's gain rule.	**10**
3	**State Variable Models:** State Transition Equation: Concept of state transition matrix, properties of state transition matrix, solution of homogeneous systems, solution of nonhomogeneous systems. Controllability and Observability: Concept of controllability, controllability analysis of LTI systems, concept of observability, observability with Examples.	**04**
4	**Stability Analysis:** Concepts of Stability and Compensators: Concept of absolute, relative and robust stability, Routh stability criterion, Lead and Lag Compensator. Root Locus Analysis: Root-locus concepts, general rules for constructing root-locus, Bode plot: Magnitude and phase plot; Method of plotting Bode plot; Stability margins on the Bode plots; Stability analysis using Bode plot. Nyquist Criterion: Polar plots, Nyquist stability criterions; Nyquist plot; Gain and phase margins.	**12**
5	**Adaptive Control Systems and Servomechanism:** Servomotors, Stepper Motors, Synchronous Motors. Optimal Control System, Adaptive control system, Basics of P, PI, and PID Controller and their applications.	**06**

List of Laboratory Experiments: (minimum eight)

1. Effect of zero and pole to the second order closed loop control system.
2. Static errors for type 0, type 1, type 2 Control System.
3. Frequency response of a 1st order and 2nd order control systems.
4. Transfer function of a 1st order and 2nd order control systems.
5. Effect of Zero and pole to open loop transfer function of a second order system with unity feedback.
6. Design root locus for given control system.
7. Design Bode plot for first and second order control system.
8. Design Nyquist plot for given control system.
9. Verification of observability and controllability for given control system.
10. Transfer functions of P, PI, and PID controller.
11. Servo mechanism and characteristics of servo motor.

Books Recommended:

Text books:

1. Nagrath, M.Gopal, *Control System Engineering*, 2nd Edn, Tata McGraw Hill.
2. K. Ogata, *Modern Control Engineering*, 3rd Edn, Pearson Publication.
3. V.K. Mehta, Rohit Mehta, *Principles of Power Systems*, 4th Edn, S. Chand publication.

Reference Books:

1. Madan Gopal, *Control Systems Principles and Design*, 7th Edn, Tata McGraw hill.
2. Normon, *Control System Engineering*, 3rd Edn, John Wiley & sons.
3. Ajit K.Mandal, *Introduction to Control Engineering*, 2nd Edn, New Age International Publication.
4. S. Hasan Saeed, *Automatic Control System*, 9th Edn, S. K. Kataria & Sons

Evaluation Scheme:
Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practicals performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments, and a case study based on any one topic is compulsory.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments, Case study): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics and Telecommunication Engineering</td><td colspan="2">Semester: V</td></tr>
<tr><td colspan="8">Course: Computer Organization & Architecture</td><td colspan="2">Course Code: DJ19ECEC5012</td></tr>
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</table>

Pre-requisite: Knowledge of

1. Digital System Design

Objectives:

1. To conceptualize the basics of organizational and architectural issues of a digital Computer.
2. To analyse performance issues in processor and memory design of a digital Computer.
3. To understand various data transfer techniques in digital computer.
4. To analyse processor performance improvement using instruction level parallelism
5. To understand different hardware techniques in ALU
6. To understand different memory organisations and mappings

Outcomes: On completion of the course, learner will be able to:

1. Demonstrate basic structure of computer and analyse its performance
2. Highlight various ALU designs and control unit designs.

3. Demonstrate implementation, Compare and contrast different Memory/IO mapping techniques.
4. Analyse instruction level parallelism with case study of 8086 processor.
5. Report and present experimental study conducted with valid conclusions

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Introduction of Computer Organization and Architecture:** Basic organization of computer, Evolution of Computers, Von Neumann model. Performance measure of Computer Architecture. Architecture of 8086 family, 8086 Hardware Design, Minimum mode & Maximum mode of Operation. Study of bus controller 8288 & its use in Maximum mode.	**06**
2	**Data Representation and Arithmetic Algorithms:** Number representation*:* Binary Data representation, two's complement representation and Floating-point representation. Integer Data arithmetic*:* Addition, Subtraction. Multiplication: Unsigned & Signed multiplication-Add & Shift Method, Booth's algorithm. Division of integers: Restoring and non-restoring division, signed division, Basics of floating point representation IEEE 754 floating point (Single & double precision) number representation. Floating point arithmetic: Addition, subtraction	**06**
3	**Control Unit:** Soft wired (Micro programmed) and hardwired control unit, Design methods. Microinstruction sequencing and execution. Micro operations, concepts of Nano programming. Introduction to RISC and CISC architectures and design issues. Introduction to parallel processing concepts, Flynn's classifications, Pipeline processing, instruction pipelining, pipeline stages, pipeline hazards. Case study: 8086	**08**
4	**Programming 8086:** Instruction formats, basic instruction cycle, Instruction interpretation and sequencing. Addressing modes, Instruction Set, Assembly Language Programming, Mixed Language Programming, Programs based on Stacks, Strings, Procedures, Macros, Timers, Counters & delay.	**10**
5	**Memory Organization:** Introduction to Memory and Memory parameters. Classifications of primary and Secondary memories. Types of RAM and ROM, Allocation policies, Memory	**06**

	Hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), Mapping techniques. Cache Coherency, Interleaved and Associative memory.	
6	**I/O Organization:** Input/output systems, I/O modules and 8089 IO processor. Types of data transfer Techniques: Programmed I/O, Interrupt driven I/O and DMA.	**06**

List of Laboratory Experiments: (minimum eight)

1. To study Full Adder (7483).
2. To study ALU (74181).
3. To study MASM (Micro Assembler).
4. Write a program for hexadecimal addition and multiplication.
5. Write a program for binary multiplication.
6. Write a program for Hamming code generation, detection and correction.
7. Write a program for Booth's multiplication
8. Write a program for LRU page replacement algorithm.
9. Write a program for FIFO page replacement algorithm.
10. Write a program to simulate the mapping techniques of Cache memory.
    - 10.1 Direct Mapped cache
    - 10.2 Associative Mapped cache
    - 10.3 Set Associative Mapped cache
11. Write a program to simulate memory allocation policies.
    - 11.1 First-fit algorithm
    - 11.2 Best-fit algorithm
12. Write a program to implement serial communication (PC - PC communication).
13. Write a program to implement parallel communication. (PC - Printer communication).
14. Write a program for printer simulation.
15. Write a program for keyboard simulation.

Books Recommended:

Text books:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, *Computer Organization*,5th Edn, Tata McGraw-Hill.
2. Douglas V Hall, *Microprocessors and Interfacing*, 3rd Edn, Tata McGraw-Hill.
3. John P. Hayes, *Computer Architecture and Organization*, 3rd Edn, Tata McGraw Hill.

4. William Stallings, *Computer Organization and Architecture: Designing for Performance* , 8th Edn, Pearson Publication.
5. B. Govindarajulu, *Computer Architecture and Organization: Design Principles and Applications*, 2nd Edn, Tata McGraw-Hill.

Reference Books:

1. Dr. M. Usha, T. S. Srikanth, *Computer System Architecture and Organization*, 1st Edn, Wiley Publication.
2. ISRD Group, *Computer Organization*, 1st Edn, Tata McGraw-Hill.
3. Y C Liu and G A Gibson, *The 8086 8088 Family, 2nd* Edn, Prentice Hall.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practicals performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
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3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments, and a case study based on any one topic is compulsory.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments, Case study): 10 marks

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Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
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</table>

Pre-requisite:

1. Analog Circuit Design
2. Digital System Design
3. Integrated Circuits

Objectives:

1. To highlight the circuit design issues in the context of VLSI technology
2. To provide understanding of VLSI circuit design using different design styles.
3. To provide introduction to HDL programming

Outcomes: At the end of course, students will be able to:

1. Understand the operation of MOSFET transistor, layout design rules and the concept of transistor scaling.
2. Analyze CMOS inverter circuit and realization of various logic circuits using different design styles. Enter the specifications in EDA tool, debug to obtain the desired result.
3. Explain operation of SRAM, DRAM, ROM memories.
4. Realize different Data path circuits using different design styles. Carry out necessary investigations on the simulated circuit, infer from the results obtained and correlate them with theoretical interpretations.

5. Simulate and synthesize digital circuits using HDL language. Report and present the experimental study conducted along with valid conclusions.

Detailed Syllabus: (unit wise)

Unit	Description	Duration
1	**MOSFET Layout and Scaling:** MOSFET Scaling: Types of scaling, short channel effects Layout: Lambda based design rules (CMOS), MOSFET capacitances.	06
2	**MOS Circuit Design Styles:** CMOS INVERTER Circuit Analysis: Static and dynamic analysis (Noise, propagation delay and power dissipation) of resistive load and CMOS inverter. Comparison of all types of MOS inverters. Design of CMOS inverters and its layout. Design styles: Static CMOS, Dynamic CMOS, pass transistor logic, transmission gate , Pseudo NMOS, Domino logic, C^2MOS, NORA logic, NP Domino logic ,Realization of Multiplexer (up to 4:1 Mux) , Encoder, Decoder, SR Latch, JK FF, D FF, 1 Bit Shift Register design in different design styles and their layouts.	14
3	**Memory and Storage circuits:** ROM array, SRAM (operation, design strategy, leakage currents, read /write circuits), layout of SRAM. DRAM (Operation of 1T, 3T, operation modes, refresh operation, Input-Output circuits), layout of DRAM.	08
4	**Data path design:** Full adder, Ripple carry adder, CLA adder, Carry Skip Adder, Carry Save Adder and carry select adder, Array Multiplier, Barrel shifter.	08
5	**Design methods:** Semi-custom Full custom design PLA PAL PROM FPGA PLD. Introduction to VHDL.	04

List of Laboratory Experiments: (minimum eight)

1. To study MOS characterization using simulation software
2. Static analysis of CMOS Inverter
3. Dynamic analysis of CMOS Inverter
4. Multiplexer design using pass transistor and transmission gate logic style
5. 1-bit CMOS Adder design using static CMOS logic style
6. 1-bit CMOS mirror Adder design
7. To write VHDL/Verilog Program for flip flops
8. To write VHDL/Verilog Program for adders
9. To write VHDL/Verilog Program for multiplexers
10. Design and simulation of barrel shifter circuit in SPICE
11. To write HDL code and simulation of barrel shifter

Books Recommended:

Text books:

1. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, 3rd Edn, Tata McGraw Hill.
2. P. Uyemura, *Introduction to VLSI Circuits and Systems*, 1st Edn, John Wiley & Sons.
3. Frank Vahid, *Digital Design with RTL design, VHDL and VERILOG*, 1st Edn, John Wiley and Sons.
4. Neil H. E. Weste, David Harris and Ayan Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd Edn, Pearson Education.
5. Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd Edn, Pearson Publication.
6. Douglas L. Perry, VHDL: Programming by Example, 4th Edn, Tata McGraw Hill.

Reference Books:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd Edn, Pearson Education.
2. Volnei A. Pedroni, *Circuit Design and Simulation with VHDL*, 2nd Edn, MIT Press.

Evaluation Scheme:

Semester End Examination (A):

Theory:

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Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester.
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Laboratory: (Term work)

Term work shall consist of minimum 8 experiments.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

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Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)

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Pre-requisite:

1. Engineering Mathematics
2. Probability theory and Random Processes

Objectives:

1. To introduce the concepts and understanding of artificial neural networks and fuzzy logic.
2. To introduce neural network design concepts
3. To expose neural networks-based methods to solve real world complex problems
4. To provide knowledge of fuzzy logic to design the real-world fuzzy systems

Outcomes: On completion of the course, learner will be able to:

1. Express Training of NN using various training rules with consideration of different parameters like overfitting, underfitting, etc.
2. Calculate and update the weights of the neural networks to specify the working and applications of different types of neural networks.
3. Design fuzzy sets for various applications and solve fuzzy set theory problems.
4. Design various engineering application using Neural Networks/ Fuzzy Logic.
5. Gain ability to work in teams to solve complex problems and communicate effectively with technical reports/ write-up.

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Introduction to Neural Networks:** Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.	**04**
2	**Essentials of Artificial Neural Networks:** Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules.	**04**
3	**Supervised Neural Networks:** Feed forward neural network, Single-Layer feed forward architecture, Multiple-Layer feed forward architecture, Types of feed forward networks, Multi-layer perceptron, Training MLP: The back-propagation algorithm, Introduction to the concept of Support Vector Machine based classifier, GRADIENT-DESCENT algorithm, Generalization, Factors to be considered, Assessing the success of learning, Metrics for evaluation of classification method, Steps to use neural networks to data, Over fitting, Detecting over fit models: Cross validation	**10**
4	**Unsupervised Learning Neural Networks:** Competitive Learning Networks – Maxnet, Mexican Hat Net, Kohonen Self-Organizing Networks – architecture, training algorithm, K-means and LMS algorithms, Radial Basis Function (RBF) neural network – architecture and algorithm, and Discrete Hopfield networks.	**10**
5	**Fuzzy logic:** Introduction to fuzzy logic, Basic Fuzzy logic theory, Fuzzy sets - properties & operations, Fuzzy relation - Operations on fuzzy relations, Fuzzy Membership functions, Fuzzy Rules and Fuzzy Reasoning, Fuzzification and Defuzzification methods, Fuzzy Inference Systems, Mamdani Fuzzy Models, Fuzzy knowledge based controllers, Sugeno Fuzzy Models.	**07**
6	**Applications of Fuzzy Logic and Fuzzy Systems:** Fuzzy pattern recognition, fuzzy C-means clustering, fuzzy image processing, Simple applications of Fuzzy knowledge based controllers like washing machines, home heating system, and train break control.	**07**

List of Laboratory Experiments: (minimum eight)

1. Fuzzy Set Operations: AND, OR, D-Morgan's theorem
2. (a)Simulation of Mamdani Fuzzy Inference System for washing machine control.
   (b) Summery of research paper based on Fuzzy logic
3. Simulation of Sugeno Fuzzy Inference System for given application
4. Simulation of Mamdani Fuzzy Inference System for image processing application. (Edge detection)
5. Write a program for perceptron training algorithm and test it for two input AND & OR gate function
6. Write a program for training and testing of Multilayer Perceptron for two input EX-OR gate
7. Write a program for training and testing of Multilayer Perceptron for character recognition application
8. Program for Radial basis neural network for interpolation application
9. Write a program for training and testing of RBF for pattern classification application
10. Kohenan Self Organising map for image classification
11. Case study.

Books Recommended:

Text books:

1. S. N. Sivanandam and S. N. Deepa *Introduction to Soft computing,* 2nd Edn, Wiley India Publication.
2. Thimothy J. Ross, *Fuzzy Logic with Engineering Applications, ,* 3rd Edn, Wiley India Publication.
3. John Yen and Reza Langari, *Fuzzy Logic- Intelligence, Control and Information,* 1st Edn, Pearson Publication.
4. S. Rajasekaran and G. A. Vijayalakshmi Pai, *Neural Networks, Fuzzy Logic, and Genetic Algorithms,* 2011 PHI.

Reference Books:

1. J. S. R. Jang, C.T. Sun, and E. Mizutani, *Neuro-Fuzzy and Soft Computing,* 1996 PHI
2. Simon Haykin, Neural Network- A Comprehensive Foundation, 1997 Pearson Education
3. J. M. Zurada, Introduction to Artificial Neural Systems, 1994 Jaico publishers
4. S. N. Sivanandam, S. Sumathi, and S. N. Deepa, *Introduction to Neural Network Using Matlab ,* 2006 Tata McGraw-Hill Publications
5. Bart Kosko, *Neural networks and Fuzzy Systems*, 1991 Pearson Education

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
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Pre-requisite:

1. C Programming.

Objectives:

1. To introduce operating system as a resource manager, its evolutions and fundamentals.
2. To help student understand concept of process and different process (linear and concurrent) Scheduling policies.
3. To help student familiar with memory, file and I/O management policies.

Outcomes: On completion of the course, learner will be able to:

1. Understand the fundamental concepts of OS.
2. Analyze the management policies adopted by processes, memory, File handling and I/O operations.
3. Apply the algorithms used for memory management, CPU scheduling and disk scheduling.
4. Apply concepts related to deadlock to solve the problems.

5. Analyze the functionalities of OS like Unix, Linux and Real Time Operating Systems

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Fundamental of Operating System (OS):** Definition, objectives, functions, evolution, services, types, and different views of OS Operating System as a resource manager, system calls, and shell, Monolithic systems, layered systems, client server model, monolithic kernel and Microkernel.	**04**
2	**Process Management and Memory Management**: Process, process creation, process control block, process states, process state transition diagram, Scheduling queues and schedulers, preemptive and non- preemptive scheduling algorithms, types of threads, multithreading models, Race condition, critical section, mutual exclusion, semaphores, monitors, Multiprogramming with fixed and variable partitions, memory allocation strategies, Logical and physical address space, paging and segmentation, Concept, performance of demand paging, page replacement algorithms, Deadlock Problem, deadlock characterization, deadlock prevention and deadlock avoidance deadlock detection and recovery	**08**
3	**File Management and Input Output Management** : File Naming, File Structure, File Types, File Access, File Attributes, File Operations, Memory Mapped Files, Implementing Files, contiguous allocation, linked list allocation, indexed allocations, Single level directory system, Two level directory system, Hierarchical Directory System, Principles of Input/output H/W: I/O Devices, Device Controllers, Direct Memory Access, Principles of Input/output S/W: Goals Of I/O S/W, Interrupt Handler, Device Driver, Device Independent I/O Software, Disks : RAID levels, Disks Arm Scheduling Algorithms, Management of free blocks.	**08**
4	**Unix Operating System**: History of UNIX, UNIX Goals, Unix Shell, interfaces to Unix, UNIX utility programs, Traditional UNIX Kernel, Modern UNIX Systems, Unix process management: Concept, Scheduling in Unix, Unix Memory management: Paging, Page replacement strategies, Unix file management: I-node, File allocation, I/O management, Unix Security measures.	**08**
5	**Linux Operating System:** History, Linux Processes and Thread management, Scheduling in Linux, Linux System calls, Memory management: Virtual memory, Buddy Algorithm, Page replacement policy,	**08**

	Linux File System, I/O management: Disk Scheduling, Advantages of Linux and Unix over Windows.	
6	**Real Time Operating System (RTOS):** Introduction, Characteristics of real-time operating systems, Real Time task Scheduling, Modeling Timing constraints, Table-driven scheduling, Cyclic schedulers, Earliest Deadline First (EDF) scheduling, Rate Monotonic Algorithm (RMA)	**04**

List of Laboratory Experiments: (minimum eight)

1. To implement linux commands.
2. To implement linux shell script.
3. To implement any one the basic commands of linux like ls, cp, mv and others using kernel APIs.
4. To implement preemptive and non-preemptive algorithms.
5. To implement concept of deadlock.
6. To implement concept of memory management.
7. To implement demand and virtual memory implementation.
8. To implement file allocation strategies.
9. To implement disk scheduling techniques.

Books Recommended:

Text books:

1. Tanenbaum, *Modern Operating Systems*, 3rd Edn, PHI Publication.
2. William Stallings, *Operating System-Internal & Design Principles*, 6th Edn, Pearson.
3. Achyut S. Godbole, *Operating Systems*, 2nd Edn, Tata McGraw Hill.

Reference books:

1. Silberschatz A., Galvin P., and Gagne G, *Operating Systems Concepts*, 8th Edn, Wiley.
2. Richard Blum and Christine Bresnahan, *Linux Command Line & Shell Scripting*, 2nd Edn, Wiley Publication.
3. Rajib Mall, *Real-Time Systems: Theory and Practice*, 1st Edn, Pearson Publication.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practical's performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments, and a case study based on any one topic is compulsory.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments, Case study): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics and Telecommunication Engineering</td><td colspan="3">Semester: V</td></tr>
<tr><td colspan="8">Course: Power Electronics</td><td colspan="3">Course Code: DJ19ECEC5016</td></tr>
<tr><td colspan="8">Course: Power Electronics- Laboratory</td><td colspan="3">Course Code: DJ19ECEL5016</td></tr>
<tr><td colspan="4" rowspan="2">Teaching Scheme (Hours / week)</td><td colspan="11">Evaluation Scheme</td></tr>
<tr><td colspan="5">Semester End Examination Marks (A)</td><td colspan="5">Continuous Assessment Marks (B)</td><td rowspan="2">Total marks (A+ B)</td></tr>
<tr><td rowspan="3">Lectures</td><td rowspan="3">Practical</td><td rowspan="3">Tutorial</td><td rowspan="3">Total Credits</td><td colspan="5">Theory</td><td>Term Test 1</td><td>Term Test 2</td><td colspan="2">Avg.</td></tr>
<tr><td colspan="5">75</td><td>25</td><td>25</td><td colspan="2">25</td><td>100</td></tr>
<tr><td colspan="5">Laboratory Examination</td><td colspan="3">Term work</td><td colspan="2" rowspan="2">Total Term work</td><td rowspan="3">50</td></tr>
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</table>

Pre-requisite:

1. Electrical Network Analysis and Synthesis
2. Analog Circuit Design

Objectives:

1. Understand power electronic devices and their characteristics.
2. Analyze power electronics-based rectifiers, inverters and choppers.

Outcomes: On completion of the course, learner will be able to:

1. Understand the functionalities of power semiconductor devices.
2. Design of triggering, commutation and protection circuits for SCRs.
3. Analyze different types of rectifiers and converters for industrial applications.
4. Analyze different types of Voltage Controllers and Cycloconvertors.
5. Gain ability to work in teams to solve complex problems and communicate effectively with technical reports / write-ups.

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Power semiconductor devices:** Principle of operation of SCR, static and dynamic characteristics, gate Characteristics. Principle of operation, characteristics, ratings and applications of: TRIAC, DIAC, MOSFET and power BJT. IGBT: basic structure, principle of operation, equivalent circuit, latch-up in IGBT's and V-I characteristics.	**08**
2	**SCR Triggering, Commutation and Protection Circuits:** Methods of turning ON SCR (types of gate signal), firing circuits (using R, RC, UJT, Ramp and pedestal, inverse cosine). Design of commutation circuits. Protection of SCR.	**08**
3	**Single-phase Controlled Rectifiers:** Introduction to uncontrolled rectifiers, Half wave controlled rectifiers with R, RL load, effect of free-wheeling diode. Full wave fully controlled rectifiers (centre-tapped, bridge configurations), full-wave half-controlled (semi-converters) with R, RL load, effect of freewheeling diode and effect of source inductance. Calculation of performance parameters, input performance parameters (input power factor, input displacement factor (DF), input current distortion factors (CDF), input current harmonic factor (HF/THD), Crest Factor (CF)), output performance parameters.	**08**
4	**Inverters:** Introduction to basic and improved series/parallel inverters, limitations. Introduction, principle of operation, performance parameters of Single-phase half / full bridge voltage source inverters with R and R-L load. Voltage control of single-phase inverters using PWM techniques, harmonic neutralization of inverters, applications.	**08**
5	**DC-DC converters:** Basic principle of step up and step-down DC-DC converters, DC-DC switching mode regulators. Buck, Boost, Buck-Boost, Cuk Regulators (CCM mode only). Voltage commutated, current commutated and load commutated DC-DC converters. Applications in SMPS, Battery charging systems. Introduction, single phase and three phase Cycloconvertors, applications	**08**

List of Laboratory Experiments: (minimum eight)

1. To study characteristics of SCR, DIAC, TRAIC.
2. To study characteristics of IGBT, MOSFET and Power BJT.
3. To implement Firing circuit for SCR using UJT.
4. To study of Half wave and Full wave rectifiers using diodes.
5. To study of half wave and Full wave controlled rectifiers.
6. To implement Buck converter, Boost converter and Buck-Boost converter.
7. To Study Cycloconvertors.
8. Simulation of single-phase half wave and Full wave rectifier circuit.
9. Simulation of controlled rectifier with R and RL load.
10. Simulation of controlled rectifier with (i) Source Inductance (ii) Freewheeling diode.

Books Recommended:

Text books:

1. M. H. Rashid, *Power Electronics: Devices, Circuits and Applications*, 4th Edn, Pearson Publication.
2. Ned Mohan, Tore M. Undeland, William P. Robbins, *Power Electronics: Converters Applications and Design*, 3rd Edn, Wiley Publication.
3. P. S. Bhimbra, *Power Electronics*, 5th Edn, Khanna Publishers.

Reference books:

1. M. D. Singh and K. B. Khanchandani, *Power Electronics*, 2nd Edn, Tata McGraw Hill
2. Ramamurthy, *An Introduction To Thyristors and Their Applications*, 2nd Edn, East-West Publication.
3. P. C. Sen, *Modern Power Electronics*, 2nd Edn, S. Chand & Company.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Laboratory:

1. Oral examination will be based on the entire syllabus including, the practical's performed during laboratory sessions.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments, and a case study based on any one topic is compulsory.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Assignments, Case study): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics & Telecommunication Engineering</td><td colspan="3">Semester: V</td></tr>
<tr><td colspan="8">Course: Data Structures & Algorithms</td><td colspan="3">Course Code: DJ19ECSBC1</td></tr>
<tr><td colspan="8">Course: Data Structures & Algorithms - Laboratory</td><td colspan="3">Course Code: DJ19ECSBL1</td></tr>
<tr><td colspan="4" rowspan="2">Teaching Scheme (Hours / week)</td><td colspan="7">Evaluation Scheme</td></tr>
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</table>

Pre-requisite:

1. Computer Programming Laboratory

Objectives:

1. Understand and remember algorithms and its analysis procedure.
2. Introduce the concept of data structures through ADT including List, Stack, and Queues.
3. To design and implement various data structure algorithms.
4. To introduce various techniques for representation of the data in the real world.
5. To develop application using data structure algorithms.
6. Compute the complexity of various algorithms.

Outcomes: On completion of the course, learner will be able to:

1. Understand and explain various data structures, related terminologies and its types
2. Select appropriate data structure and apply it to solve problems in various domains
3. Understand and Implement appropriate sorting and searching algorithm for a given problem statement and analyze its complexity

4. Understand the concepts of trees and graphs in real life problem solving

Detailed Syllabus: (unit wise)		
Unit	**Description**	**Duration**
1	**Introduction to Data structures and Algorithms:** Introduction to Data structures, Need of Data structures, Types of Data structures : Linear and nonlinear data structures Arrays, Stacks, Queue, Linked list and Tree, Graph, Recursion, ADT (Abstract Data type). Introduction to Analysis, Algorithms, characteristics of an algorithms, Time and Space complexities, Order of growth functions, Asymptotic notations	**06**
2	**Stack:** Introduction to Stack, Stack as ADT, Operations on stack, Application of stack: – reversing string, Polish notations	**06**
3	**Queue:** Introduction to Queue, Queue as ADT, Operations on Queue, Linear representation of queue, Circular Queue, Priority Queue, De-queue, Application of Queues	**04**
4	**Linked List:** Introduction to Linked List, Basic concept of Linked List, Memory allocation & de allocation of Linked list, Singly Linked list, Doubly Linked list, Circular linked list, Operations on linked list, Linked representation of stack, Linked representation of Queue, Application of linked list.	**08**
5	**Sorting and Searching:** Introduction to Sorting: Bubble Sort, Selection Sort, Insertion Sort, Quick Sort, Merge Sort, Heap Sort, Shell Sort, Radix sort. Analysis of Sorting Techniques. Comparison of sorting Techniques Introduction to Searching: Linear search, Binary search, Hashing Techniques, Different Hash functions, Collision& Collision resolution techniques, Analysis of searching Techniques.	**08**
6	**Trees & Graph:** Introduction to Trees, Definitions & Tree terminologies, Binary tree representation, Operations on binary tree, Traversal of binary trees, Binary search tree, Threaded Binary tree, Expression tree, Application of Trees Introduction to Graph, Introduction Graph Terminologies, Graph Representation, Type of graphs, Graph traversal: Depth first search(DFS) & Breadth First search(BFS), Minimum Spanning Tree : Prim's & Kruskal's Shortest Path Algorithm – Dijkstra's Algorithm. Applications of graph	**10**

List of Laboratory Experiments:

1. WAP to implement stack menu driven program.
2. WAP to implement Infix to Postfix Transformation and its evaluation program.
3. WAP to implement double ended queue menu driven program.
4. WAP to implement different operations on linked list –copy, concatenate, split, reverse, and count no. of nodes.
5. WAP to implement construction of expression tree using postfix expression.
6. WAP to implement Quick Sort, Merge sort and Heap Sort menu driven program.
7. WAP to implement hashing functions with different collision resolution techniques.

Books Recommended:

Text books:

1. Tenenbaum, Langsam, Augenstein, *Data structures using C*, 7th Edn, 2009, Pearson.
2. Reema Thareja, *Data Structures using C*, 2011, Oxford University Press.
3. P.S.Deshpande, O.G.Kakde, *C and Data structures*, 2003, Dreamtech Press.
4. Jean-Paul Tremblay, Paul G. Sorenson, P. G. Sorenson, *An Introduction to Data Structure with Applications*, 1984, McGraw-Hill.

Reference Books:

1. Rajesh K. Shukla ,*Data Structures Using C & C++*, 2009, Wiley India.
2. Mark A.Weiss, *Data Structures and Algorithm Analysis in C*, 2014, Pearson.
3. Harsh Bhasin, *ALGORITHMS Design and Analysis*, 2015 Oxford University Press.
4. Ellis Horowitz and Sartaj Sahni, *Computer Algorithms*, 1978, Computer Science Press.

Evaluation Scheme:

Semester End Examination (A):

Theory:

1. Question paper based on the entire syllabus will comprise of 5 questions (All compulsory, but with internal choice as appropriate), each carrying 15 marks, total summing up to 75 marks.
2. Total duration allotted for writing the paper is 3 hrs.

Continuous Assessment (B):

Theory:

1. Two term tests of 25 marks each will be conducted during the semester out of which; one will be a compulsory term test (on minimum 02 Modules) and the other can either be a term test or an assignment on live problems or a course project.
2. Total duration allotted for writing each of the paper is 1 hr.
3. Average of the marks scored in both the two tests will be considered for final grading.

Laboratory: (Term work)

1. Term work shall consist of minimum 7 experiments, 1 Power Point Presentation and minimum 2 assignments.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-up, Power Point Presentation and Assignments: 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics & Telecommunication Engineering</td><td colspan="3">Semester: V</td></tr>
<tr><td colspan="8">Course: Database Management System - Laboratory</td><td colspan="3">Course Code: DJ19ECSBL2</td></tr>
<tr><td colspan="4" rowspan="2">Teaching Scheme (Hours / week)</td><td colspan="7">Evaluation Scheme</td></tr>
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</table>

Pre-requisite:

1. Computer Programming

Objectives:

1. Learn and practice data modeling using the entity-relationship and developing database designs.
2. Understand the use of Structured Query Language (SQL) and learn SQL syntax.

Outcomes: On completion of the course, learner will be able to:

1. Analyze a case study and create ER diagram of the scenario and able to create Database schema from this using given software and SQL.
2. Write basic SQL queries to apply constraints, insert rows, do basic operations like alter, update and delete, to use basic aggregate functions and retrieve information from databases.
3. Perform normalization on tables by analyzing functional dependencies.
4. Write SQL queries to make joins and views on table.
5. Perform nested queries and triggers.

List of Laboratory Experiments: (minimum eight)

Experiments are be based on theory topics given below.

Introduction to Databases:

Characteristics of databases, Users of Database system, Database architecture, Data abstraction, Different data models.

The Entity-Relationship (ER) Model:

Types of entities and Attributes, Keys, Relationship constraints: Cardinality and Participation.

Relational Database:

Relational schema and concept of keys, Mapping ER model to Relational Model, Constraints, types of constrains, Integrity constraints, Normalization 1NF,2NF,3NF,BCNF.

1. Identify the case study and detail statement of problem. Design an Entity-Relationship (ER) model.
2. Convert the designed ER model to a Relational Database and create required tables (DATA DEFINITION STATEMENTS) and apply the constraints like Primary Key, Foreign key, NOT NULL to the tables.

SQL:

SQL Data Definition and Data Types, Specifying Constraints in SQL, Basic Retrieval Queries in SQL, INSERT, DELETE, and UPDATE Statements in SQL, Views (Virtual Tables) in SQL, aggregate functions, nested sub queries, JOINTS, Triggers.

3. Write SQL statements for inserting rows (INSERT) and implementing ALTER, UPDATE and DELETE.
4. Perform following aggregate functions: MAX (), MIN (), AVG (), COUNT ().
5. Identify dependencies in a table and accordingly convert it to 1NF, 2NF, 3NF and BCNF.
6. Perform SELECT statement for retrieval of data from Database.
7. Perform various JOIN operations on Tables.
8. Create views and access data from it using SQL statements.
9. Perform queries for triggers.
10. Perform Nested queries.
11. Case study.

Books Recommended:

Text Books:

1. A.Silberschatz, H.Korth, S.Sudarshan, *Database System and Concepts*, 5th Edn, McGraw-Hill.
2. Rob, Coronel, *Database Systems*, 7th Edn, Cengage Learning.
3. Ramez Elmasri, Shamkant, B. Navathe, *Fundamentals of Database System*, 7th Edn, Person.
4. G. K. Gupta, *Database Management Systems*, 1th Edn, McGraw – Hill.

Reference Books:

1. Peter Rob, Carlos, Coronel, *Database Systems Design Implementation and Management*, 5th Edn, Thomson Learning.
2. Mark L. Gillenson, Paulraj Ponniah, *Introduction to Database Management*, 1st Edn, Wiley.
3. Raghu Ramkrishnan, Johannes Gehrke, *Database Management Systems*, 3rd Edn, Tata McGraw-Hill.

Evaluation Scheme:

Continuous Assessment:

Laboratory: (Term work)

1. Term work shall consist of minimum 8 experiments and one case study.

The distribution of marks for term work shall be as follows:

i. Laboratory work (Performance of Experiments): 15 Marks
ii. Journal Documentation (Write-ups, Case study): 10 marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

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Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year B.Tech. in Electronics and Telecommunication</td><td colspan="3">Semester: V</td></tr>
<tr><td colspan="8">Course: Professional & Business Communication Laboratory</td><td colspan="3">Course Code: DJ19IHL2</td></tr>
<tr><td colspan="4" rowspan="2">Teaching Scheme (Hours / week)</td><td colspan="7">Evaluation Scheme</td></tr>
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</table>

*2 hrs. Theory (Class wise) and 2 hrs. Tutorial (Batch wise)

Pre-requisite:

1. Basic course in Effective Communication Skills

Objectives:

1. To inculcate professional and ethical attitude at the workplace
2. To enhance communication and interpersonal skills
3. To develop effective presentation skills
4. To hone written skills for technical documentation

Outcomes: On completion of the course, learner will be able to:

1. Plan, organize and write technical documents like reports, proposals and research papers in the prescribed format using appropriate language and style with an understanding of ethics in written communication
2. Apply techniques of writing resume, participating in a group discussion and facing interviews
3. Develop interpersonal skills in professional and personal situations

4. Understand the documentation process of meetings and conduct meetings in a professional manner
5. Understand communication across cultures and work ethics
6. Design and deliver effective presentations using Power Point

Detailed Syllabus: (unit wise)

Unit	Description	Duration
1	**Technical Writing** : Report Writing: Types of report, parts of formal report, collection of data and survey analysis, pre-writing of report, language and style in reports, formatting of reports, referencing in report Proposal Writing: Types of technical proposals, format of proposal, language and style, presentation of proposal. Technical Paper Writing: Parts of a technical paper, language and formatting, referencing in IEEE format. Plagiarism: Types of plagiarism, consequences of plagiarism.	**08**
2	**Employment Skills Group Discussion:** Purpose of a GD, types of GD, criteria for evaluating a GD, Dos and Don'ts of a GD, Tips to be successful in GD. Cover Letter & Resume Writing: Format and content of cover letter, types of resume, structure, content and formatting of resume. Interview Skills: Types and modes of interview, Preparation for interview, Dos and Don'ts of interview, frequently asked questions during interview.	**06**
3	**Introduction to Interpersonal Skills**: Emotional Intelligence: Definition, difference between IQ and EQ, how to develop EQ. Leadership: Types of leadership, leadership styles, case studies. Team Building: Difference between group and team, importance of team work, strategies to be a good team player. Time Management: Importance of time management, cultural views of time, 80/20 rule, time wasters, setting priorities and goals. Conflict Management: Types of conflicts, strategies to manage conflict, case studies.	**05**
4	**Meetings and Documentation**: Planning and preparation for meetings, strategies for conducting effective meetings, notice, agenda and minutes of a meeting, business meeting etiquettes	**02**

5	**Cross-cultural communication and Ethics**: Communication across cultures, professional and work ethics, responsible use of social media, introduction to Intellectual Property Rights.	**03**
6	**Presentation Skills:** Presentation strategies, overcoming stage fear, techniques to prepare effective PowerPoint presentation	**02**

List of Assignments:

1. Business Proposal (PowerPoint presentation).
2. Resume writing.
3. Interpersonal Skills (documentation of activity).
4. Meetings and Documentation (Notice, Agenda, Minutes of Mock Meetings).
5. Business ethics.
6. Presentation Skills.

Books Recommended:

Reference Books

1. Fred Luthans, *Organizational Behavior,* 12th Edn, McGraw Hill.
2. Lesiker and Petit, *Report Writing for Business*, McGraw Hill, 1997.
3. Huckin and Olsen, *Technical Writing and Professional Communication,* McGraw Hill, 1991.
4. Wallace and Masters, *Personal Development for Life and Work*, 12th Edn. Thomson Learning.
5. Heta Murphy, *Effective Business Communication*, Mc Graw Hill, 2017.
6. R.C. Sharma and Krishna Mohan, *Business Correspondence and Report Writing*, Tata McGraw-Hill Education, 2017.
7. B. N. Ghosh, *Managing Soft Skills for Personality Development,* Tata McGraw Hill, 2012.
8. Arthur H. Bell, Dayle M. Smith, *Management Communication*, 3rd Edn, Wiley India Edition, 2010.
9. Dr. K. Alex, *Soft Skills*, S Chand and Company, 2009.
10. R. Subramaniam, *Professional Ethics*, Oxford University Press, 2013.

Evaluation Scheme:

Laboratory: (Term work)

Term work shall consist of 6 assignments, Group Discussion and Power Point Presentation based on the written report

The distribution of marks for term work shall be as follows:

Assignments …… (25) Marks

Project Report and Presentation…… (15) Marks

Group Discussion……. (10) Marks

TOTAL: …….. (50) Marks

The final certification and acceptance of term work will be subject to satisfactory performance of laboratory work and upon fulfilling minimum passing criteria in the term work.

Prepared by Checked by Head of the Department Principal

Syllabus for Third Year Electronics and Telecommunication Engineering-Semester V (Autonomous)
(Academic Year 2021-2022)

<table>
<tr><td colspan="8">Program: Third Year Electronics & Telecommunication Engineering</td><td colspan="3">Semester : V</td></tr>
<tr><td colspan="8">Course : Innovative Product Development-III</td><td colspan="3">Course Code: DJ19ILL1</td></tr>
<tr><td colspan="4" rowspan="3">Teaching Scheme
(Hours / week)</td><td colspan="7">Evaluation Scheme</td></tr>
<tr><td colspan="4">Semester End Examination Marks (A)</td><td colspan="3">Continuous Assessment Marks (B)</td><td rowspan="2">Total marks (A+ B)</td></tr>
<tr><td rowspan="3">Lectures</td><td rowspan="3">Practical</td><td rowspan="3">Tutorial</td><td rowspan="3">Total Credits</td><td colspan="4">Theory</td><td>Term Test 1</td><td>Term Test 2</td><td>Avg.</td></tr>
<tr><td colspan="4">--</td><td>--</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td colspan="4">Laboratory Examination</td><td colspan="2">Term work</td><td rowspan="2">Term work Avg.</td><td rowspan="3">50</td></tr>
<tr><td rowspan="2">--</td><td rowspan="2">2</td><td rowspan="2">--</td><td rowspan="2">1</td><td>Oral</td><td>Practical</td><td>Oral & Practical</td><td>Review 1</td><td>Review 2</td></tr>
<tr><td>--</td><td>--</td><td>25</td><td>25</td><td>25</td><td>25</td></tr>
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Pre requisite:

1. Analog and Digital Circuits
2. Analog Communication
3. Basic Programming Skills

Objectives:

1. To determine the goals, resource requirements of project and produce them in the form of documentation.
2. To learn effective utilization of time and project management skills.
3. To address the real-world projects, to connect theory with practice as per recent industrial trends.
4. To integrate knowledge and skills from various areas through more complex and multidisciplinary projects.

Outcomes: On completion of the course, learner will be able to:

1. Identify various approaches to complete a project.
2. Demonstrate project work by considering scope, time, costs and quality
3. Pursue a collaborative project environment with team members.
4. Demonstrate the survey of several available literatures in the preferred field of study.
5. Improve the software/ hardware skills, problem solving skills, conceptual skills and communication skills.

Syllabus: Domain knowledge (any beyond) needed from the following areas for the effective implementation of the

project:

Microcontroller and Embedded Systems, Signal Processing, Microwave and Antennas, Networking and Internet of Things, Data science and Big data, Communication, Web and Application development, Robotics, AI and Machine learning, etc.

The above areas can be updated based on the technological innovations and development needed for specific project.

Guidelines: The main purpose of this activity is to improve the students' documentation and technical skills to find the cost effective solution. Guidelines are as follows:

1. The project work is to be carried out by a group of 4/5/6 students(2/3 second year and 2/3 third year students)
2. Each group is allotted a final year student as mentor and a faculty member as guide.
3. Project topics will be floated in various domains. Each group submits three project topic preferences, out of which one topic is allotted in discussion with faculty guide and faculty coordinators.
4. Each group will identify the hardware and software requirement for their problem statement.
5. Each group will be reviewed twice in a semester (August and October) and marks will be allotted based on the various points mentioned in the evaluation scheme.
6. In the first review of this semester, each group is expected to complete the literature survey, budget plan and documentation based on project methodology.
7. In the second review of this semester, each group is expected to complete 30% of project.
8. Subsequent reviews will be carried out in sixth semester.

Evaluation Scheme:
Semester End Examination (A):

Laboratory:
Oral examination should be conducted by Internal and External examiners. Students have to give presentation and demonstration based on their project.

Continuous Assessment (B):
Laboratory: (Term work)
Each group will be reviewed twice in a semester by faculty guide and faculty coordinators based on the following criteria:

1. Objective and expected outcome
2. Long term social impact
3. Innovative ideas and motivation

4. Documentation
5. Simulation effectiveness
6. Literature survey and comparative research methodology
7. Project Progress/Implementation
8. Overall Presentation and team work

Each review consists of 25 marks. Average of the marks scored in both the reviews will be considered for final grading. The final certification and acceptance of TW ensures the satisfactory performance on the above aspects.

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